REMARKS

Claims 1–20 are pending in the present application.

Claim 19 was amended herein.

Reconsideration of the claims is respectfully requested.

37 C.F.R § 1.83(a) (Drawings)

The drawings were objected to under 37 C.F.R. § 1.83(a) as failing to show every feature of the invention. This object is respectfully traversed.

The Office Action asserts that the limitation of a "pulsed bias current compris[ing] a pulse at one edge of a system clock" in claims 7 and 15 is not shown in the drawings. However, FIGURES 2B and 2C include a depiction of the voltage at the node ngain depicted in FIGURE 1, which is representative of the bias current ibias in FIGURE 1. The signal is pulsed, with the system clock period being implicitly depicted by the spacing between pulses.

The Office Action also asserts that the limitation of "an output of the comparator [being] sampled at another edge of the system clock" in claims 7 and 15 is not shown in the drawings. However, FIGURES 2B and 2C include a depiction of the voltage at the output out depicted in FIGURE 1. Again, the signal is pulsed, and the system clock is implicitly depicted by the spacing between pulses.

The Office Action still further asserts that the limitation of "a current source biased by the pulsed or continuous bias current and controlled by the input signal" in claim 19 is not shown in the

drawings. Claim 19 has been amended to correct this error. As depicted in FIGURE 1, the first or input gain stage 101 may include a current source I1 producing the bias current and controlled by an input signal gm.

Therefore, the objection to the drawings under 37 C.F.R. § 1.83(a) has been overcome.

35 U.S.C. § 112, First Paragraph (Enablement)

Claims 7–8 and 15–20 were rejected under 35 U.S.C. § 112, first paragraph as containing subject matter that was not described in the specification in such a way as to enable one skilled in the art to make and use the invention. This rejection is respectfully traversed.

The Patent Office bears the initial burden of establishing a reasonable basis for questioning enablement. MPEP § 2164.04, p. 2100-189 (8th ed. rev. 2 May 2004). The Office Action essential contends that subject matter not explicitly depicted in the drawings–such as a system clock signal, edge-triggered responses to the clock signal, and operating in different modes–is not enabled. However, such features are commonly found in the art, and are well within the purview of those of ordinary skill in the art to implement without undue experimentation.

Therefore, the rejection of claims 7–8 and 15–20 under 35 U.S.C. § 112, first paragraph has been overcome.

35 U.S.C. § 102 (Anticipation)

Claims 1–3 and 9–11 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,708,673 to *Ikeuchi*. Claims 1–4, 6, 9–12 and 14 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,708,673 to *Ikeuchi*. Claims 1 8–9 and 16–19 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Application Publication No. 2004/0164802 to *Hughes*. This rejection is respectfully traversed.

A claim is anticipated only if each and every element is found, either expressly or inherently described, in a single prior art reference. The identical invention must be shown in as complete detail as is contained in the claim. MPEP § 2131 at p. 2100-73 (8th ed. rev. 2 May 2004).

Independent claims 1 and 9 each recite an input gain stage biased with a pulsed bias current. Such a feature is not found in the cited references. *Ikeuchi* teaches a controller 6 controlling the bias current and a separate controller 7 controlling (output) pulse current. *Ikeuchi* contains no teaching or suggestion that the bias current is pulsed. *To et al* teaches a selectively variable (rather than fixed) bias current, but does not suggest that the bias current be pulsed rather than constant at a selected level. Similarly, *Hughes* also teaches that the bias current is selectively variable rather than fixed, but does not suggest a pulsed bias current rather than a constant bias current at a selected level.

Independent claim 17 recites that the input gain stage bias current is selectively either oulsed or continuous (constant). Such a feature is not shown in the cited reference. As noted above,

Hughes teaches that the bias current is selectively variable rather than fixed, but does not suggest a pulsed bias current rather than a constant bias current at a selected level.

Therefore, the rejection of claims 1–4, 6, 8–12, 14 and 16–19 has been overcome.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***wmunck@davismunck.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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